Claims

1. A System-on-Chip (SOC) apparatus, comprising:

a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller;

a first internal unidirectional bus that couples to said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred.

2. An apparatus according to claim 1, wherein said single semiconductor integrated circuit further comprises:

one or more non-DMA peripherals; and

a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, and said non-DMA peripheral(s) using unidirectional address and transaction control signals.

3. A System-on-Chip (SOC) system, comprising:

a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller;

a first internal unidirectional bus that couples to said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred.

4. A system according to claim 3, wherein said single semiconductor integrated circuit further comprises:

one or more non-DMA peripherals; and

a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, and said non-DMA peripheral(s) using unidirectional address and transaction control signals.

5. A method that makes a System-on-Chip (SOC) apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller; and

coupling a first internal unidirectional bus to said one or more processor subsystems, to said Memory Access Controller, and to and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred.

6. A method according to claim 5, wherein said single semiconductor integrated circuit further comprises:

one or more non-DMA peripherals; and

a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, and said non-DMA peripheral(s) using unidirectional address and transaction control signals.

7. A method that uses a System-on-Chip (SOC) apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller;

carrying unidirectional address and transaction control signals on a first internal unidirectional bus coupled to said one or more processor subsystems, to said Memory

Access Controller, and to and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred.

8. A method according to claim 7, wherein said single semiconductor integrated circuit further comprises one or more non-DMA peripherals and said method further comprises:

carrying unidirectional address and transaction control signals on a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems and said non-DMA peripheral(s).

9. A dependent claim according to claim 1, 2, 3, 4, 5, 6, 7, or 8, wherein said single semiconductor integrated circuit further includes a bus arbiter coupled to said first internal unidirectional bus, wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus.

10. A dependent claim according to claim 9, wherein said memory access arbitration for a selected transaction either overlaps a data transfer associated with a prior

transaction, or occurs in the same clock cycle in which access is granted and data transfer begins for said selected transaction.

11. A dependent claim according to claim 1, 2, 3, 4, 5, 6, 7, or 8 wherein said first internal unidirectional bus supports reading and writing data in bursts.

12. A dependent claim according to claim 1, 2, 3, 4, 5, 6, 7, or 8, wherein a variable number of clock cycles elapse between any two said pipelined memory transactions.

13. A dependent claim according to claim 1, 3, 5, or 7 wherein one or more of said DMA-type peripherals use one of the following clock signals: a clock signal having a frequency that is different from the first internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the first internal unidirectional bus clock signal, but has a different time domain than the first internal unidirectional bus clock signal.

14. A dependent claim according to claim 2, 4, 6, or 8 wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.

15. A System-on-Chip (SOC) apparatus, comprising:

a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, one or more non-DMA peripherals, and a Memory Access Controller;

a first internal unidirectional bus that couples to said one or more processor

subsystems, said Memory Access Controller, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports reading and writing data in bursts and supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred and said first internal unidirectional bus;

a bus arbiter coupled to said first internal unidirectional bus, wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus; and

a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, and said non-DMA peripheral(s) using unidirectional address and transaction control signals, wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.

16. A System-on-Chip (SOC) system, comprising:

a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, one or more non-DMA peripherals, and a Memory Access Controller;

a first internal unidirectional bus that couples to said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports reading and writing data in bursts and supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred and said first internal unidirectional bus;

a bus arbiter coupled to said first internal unidirectional bus, wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus; and

a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, and said non-DMA peripheral(s) using unidirectional address and transaction control signals, wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a

clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.

17. A method that makes a System-on-Chip (SOC) apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, one or more non-DMA peripherals, and a Memory Access Controller;

coupling a first internal unidirectional bus to said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports reading and writing data in bursts and supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred and said first internal unidirectional bus;

coupling a bus arbiter to said first internal unidirectional bus, wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus; and

providing a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and controls transactions between

said one or more processor subsystems, and said non-DMA peripheral(s) using unidirectional address and transaction control signals, wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.

18. A method that uses a System-on-Chip (SOC) apparatus, comprising:

providing a single semiconductor integrated circuit that includes one or more processor subsystems, one or more DMA-type peripherals, one or more non-DMA peripherals, and a Memory Access Controller;

controlling transactions between said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s) using a first internal unidirectional bus that couples to said one or more processor subsystems, said Memory Access Controller, and said DMA-type peripheral(s), said first internal unidirectional bus has a clock signal and uses a single centralized address decoder and unidirectional address and transaction control signals launched and captured on the rising edges of the clock signal, said first internal unidirectional bus supports reading and writing data in bursts and supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred and said first internal unidirectional bus;

granting access to said first internal unidirectional bus and arbitrating memory accesses for transactions on said first internal unidirectional bus using a bus arbiter

coupled to said first internal unidirectional bus; and

controlling transactions between said one or more processor subsystems, and said non-DMA peripheral(s) using a second internal unidirectional bus that couples said one or more processor subsystems via an interface controller to said non-DMA peripherals, said second internal unidirectional bus has a clock signal and uses unidirectional address and transaction control signals, wherein one or more of said non-DMA peripherals use one of the following clock signals: a clock signal having a frequency that is different from the second internal unidirectional bus clock signal, or a clock signal having a frequency that is the same as the frequency of the second internal unidirectional bus clock signal, but has a different time domain than the second internal unidirectional bus clock signal.